REMARKS

For purposes of expediting prosecution, claim 1 is amended to include the limitations of claim 2, which is now cancelled, and independent claim 17 is amended to include the limitations of claim 18, which is also now cancelled. Claims 3 and 19 are amended to clarify the invention. Claims 1, 3-17, and 19-31 remain for consideration, and reconsideration and allowance are respectfully requested.

The rejection of claims 1 and 12-17 under 35 USC §103(a) over "Quayle" (US Patent No. 6,694,464 to Quayle et al.) in view of "Nishihara" (US Patent No. 6,304,101 to Nishihara) is respectfully traversed because the Office Action fails to show that all the limitations are suggested by the references and fails to provide a proper motivation for modifying the teachings of Quayle with teachings of Nishihara. However, the rejection of the claims is now moot in view of the amendments to claims 1 and 17.

Claim 1 is amended to include limitations from claim 2 of a mask memory specifying variant memory cells of the configuration memory, wherein a value in a variant memory cell is permitted to vary during operation of the PLD; and a mask circuit coupled to the mask memory and to the buffer circuit and arranged to substitute in the blocks of data a constant value for the value of each variant memory cell. Claim 17 is similarly amended. The combination of these limitations and the other limitations is not shown to be suggested by the Quayle-Nishihara combination. Furthermore, as explained below the other combinations of references are not shown to suggest this combination of limitations.

The alleged motivation for combining Nishihara with Quayle is unsupported by evidence. The alleged motivation states that "it would have been obvious ... to enable the frame circuit to retrieve data from each column of the configuration memory as doing so would enable the invention to test in a more quick and efficient manner." This alleged motivation is unfounded because Quayle's frames are apparently unrelated to frames of data from programmable logic devices. Rather, in Quayle's system, "a frame is generated following each trace clock 2002 and consists of all the data shifted out once for the logic chip 10 or 204 scan chains ... and may fill from two to sixty-four RAM locations." (col. 27, l. 37-45) Thus, Quayle's frames are unrelated

to PLD frames, and Quayle would have no apparent reason to utilize Nishhara's approach.

The rejection of claims 1 and 12-17 should be withdrawn because a *prima facie* case of obviousness has not been established.

The Office Action fails to establish that claims 2-4, 6, 10 and 11 are unpatentable under 35 USC §103(a) over the Quayle-Nishihara combination and further in view of "Raza" (US Patent No. 5,943,488 to Raza). The rejection is respectfully traversed because the Office Action fails to show that all the limitations are suggested by the references and fails to provide a proper motivation for modifying the teachings of the Quayle-Nishihara combination with teachings of Raza.

The limitations of claim 2, which are now included in claim 1, include a mask memory specifying variant memory cells of the configuration memory, wherein a value in a variant memory cell is permitted to vary during operation of the PLD; and a mask circuit coupled to the mask memory and to the buffer circuit and arranged to substitute in the blocks of data a constant value for the value of each variant memory cell. The cited portions of Raza neither teach nor suggest these limitations.

The limitations clearly indicate that a variant memory cell is one in which the value varies during operation of the PLD. None of the cited teachings of Raza suggest that the value in a cell varies during operation. Furthermore, none of the cited portions in any apparent manner suggests any substitution of a constant value in a block of data that is assembled for error checking for each variant memory cell. Raza is directed to generating a masked programmed device by mask programming interconnects (Abstract). Thus, there is no apparent relevance to the particular claim limitations.

The alleged motivation for combining Raza with the Quayle-Nishihara combination is unsupported by evidence and improper. The alleged motivation states that "it would have been obvious ... to include a mask memory and have mask programmable chips, since one of ordinary skill in the art would have realized that using mask memory concerns a method of quickly and efficiently producing a mask programmed PLD..." However, Raza's explicit teachings appear to teach away from making the combination. Specifically, Raza teaches that "it is desirable to have a

device that occupies a smaller die area[, and] this may be accomplished by reducing and/or eliminating programming and/or testing circuitry in the device." (col. 1, l. 66 – col. 2, l. 2) Since Quayle's method and apparatus are directed dynamically testing interconnect (Title and Abstract), there would be no reasonable motivation for one to use Raza's approach for generating a masked programmable device in Quayle's system. Therefore, the alleged motivation is improper.

The Office Action also fails to show that the limitations of claim 3 are suggested by the Quayle-Nishihara-Raza combination. That is, the cited portions of Raza make no apparent suggestion that a mask circuit is inhibits modification of the value of variant memory cells during updates to the configuration memory with a corrected block of data. Raza's masking does not appear to inhibit any configuration, nor does Raza's masking have any apparent relevance to inhibiting modification during an update with a corrected block of data. Thus, the claim 3 limitations are not shown to be suggested by the prior art.

Claims 4, 6, and 10 depended from claim 1 through claim 2, and are not shown to be unpatentable for at least the reasons set forth above.

The limitations of claim 11 are not shown to be suggested by the Quayle-Nishihara-Raza combination. Claim 11 further sets forth that the check circuit is further arranged to indicate in the plurality of storage elements respective numbers of detected correctable errors and detected uncorrectable errors. The Office Action admits that none of the references explicitly teach these limitations. Furthermore, the Office Action does not provide any evidence that motivates the storage of respective numbers of detected correctable errors and detected uncorrectable errors. Therefore, the rejection of claim 10 is improper.

The rejection of claims 2-4, 6, 10 and 11 over the Quayle-Nishihara-Raza combination should be withdrawn because a *prima facie* case of obviousness has not been established.

The rejection of claims 5 and 7-9 under 35 USC §103(a) over the Quayle-Nishihara-Raza combination and further in view of "Sinha" (US Patent No. 6,378,101 to Sinha) is respectfully traversed because the Office Action does not show that all the limitations are suggested by the references and does not provide a proper motivation

for modifying the teachings of the Quayle-Nishihara-Raza combination with teachings of Sinha.

The limitations of claims 5 and 7-9 are not shown to be suggested by the prior art for at least the reasons set forth above for the base claims 1-4. Furthermore, the alleged motivation is unsupported by evidence and improper. Therefore, the rejection of claims 5 and 7-9 should be withdrawn.

The rejection of claims 18-31 is improper and should be withdrawn for at least the reasons set forth above for claims 1-17.

CONCLUSION

Reconsideration and a notice of allowance are respectfully requested in view of the Remarks presented above. If the Examiner has any questions or concerns, a telephone call to the undersigned is invited.

Respectfully submitted,

Kim Kanzaki, Ph.D.
Attorney for Applicants
Reg. No. 37,652

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on June 14, 2006.

Pat Tompkins
Name

Pat Tompkins
Signature